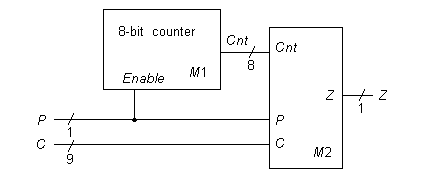
**ISCAS-89 s208.1 Frequency Divider**



**Statistics:** 10 inputs; 1 output; 112 gates;

**Function:** The functional model for the s208.1 frequency divider (also called a fractional multiplier) is shown in above. The control lines C determine if the P input pulse train is passed to the output Z, or if a frequency-divided version is passed. For every N input pulses on P, there are N\*C/256 pulses on Z. If C equals 256, all pulses on P are passed to Z.

**Models:**

* [s208.1 ISCAS-89 netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s208.1.isc)
* [s208.1 Verilog hierarchical structural model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s208.1.v)
* [s208.1 Verilog hierarchical behavioral model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s208.1b.v)
* [s208.1 complete gate-level tests](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/s208.1.tests)